

**AMENDMENTS TO THE SPECIFICATION:**

Replace the paragraph at page 2, beginning at line 24, with the following amended paragraph:

a1  
A REAL™ DSP available from Phillips Philips Semiconductor features a dual Harvard architecture with two 16-bit data buses connected to a data-computation unit (DCU). Each ALU in the DCU operates on 32-bit data and eight overflow bits and stores the results in four, 40-bit accumulators. A feature of this DSP is that each 32-bit ALU may be split into two 16-bit ALUs.

Replace the paragraph at page 16, Abstract of the Disclosure, with the following amended paragraph:

a2  
A data processor, such as a DSP, includes a multiplier block having a multiplier front end for generating partial products from input operands, and further includes a plurality of ALUs having inputs that are switchably or programmably coupled, in a first mode of operation, to first data sources representing outputs of the multiplier front end. In the first mode of operation the ALUs add together partial products received from the multiplier front end to arrive at a multiplication result. In a second mode of operation the inputs of the plurality of ALUs are switchably or programmably coupled to second data sources for performing at least one of arithmetic and logical operations on data received from the second data sources. ~~In this case the plurality of ALUs can operate together in parallel. In general, the partial products have a width of n-bits, and a width of the ALUs is one of n-bits or less than n-bits. For example, the partial products have a width of 8-bits, and the width of the ALUs is one of 8-bits or 4-bits. At least for the case where the width of the ALUs is less than n-bits, at least some of the plurality of ALUs are switchably or programmably coupled together to provide an n-bit wide ALU. In the preferred embodiment the DSP forms a part of a wireless terminal, such as a cellular telephone.~~